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FIBER OPTICS USE IN THE P-3C AIRCRAFT. A FIBER OPTIC INTERCONNE--ETC(U)
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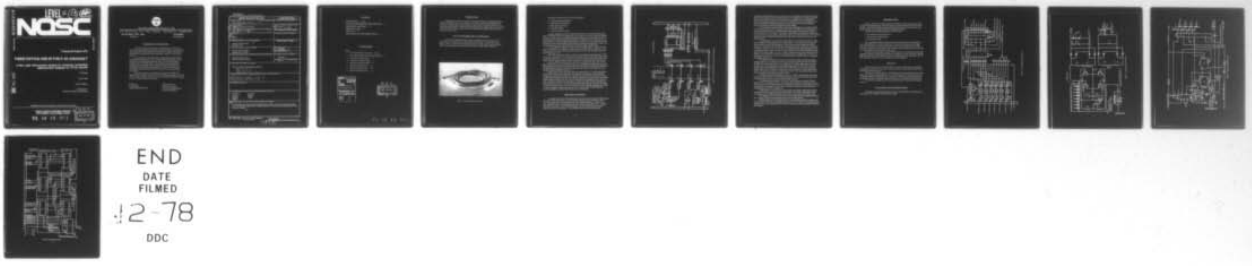

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Technical Report 272

FIBER OPTICS USE IN THE P-3C AIRCRAFT

A fiber optic interconnect system for computer controlled alphanumeric displays in a P-3C aircraft

A Flores

1 May 1978

Interim Report

Prepared for
Naval Air Systems Command

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NAVAL OCEAN SYSTEMS CENTER
SAN DIEGO, CALIFORNIA 92152

NAVAL OCEAN SYSTEMS CENTER, SAN DIEGO, CA 92152

AN ACTIVITY OF THE NAVAL MATERIAL COMMAND

RR GAVAZZI, CAPT USN
Commander

HL BLOOD
Technical Director

ADMINISTRATIVE INFORMATION

The Naval Ocean Systems Center was tasked in early FY76, by the Naval Air Systems Command, to develop, install and evaluate a prototype fiber optic interconnect link for installation aboard a P-3C aircraft to demonstrate the feasibility of applying fiber optic technology to future P-3C aircraft production.

A prototype fiber optic interconnect was developed, under contract, by Lockheed to interface the CP-901 computer data processing unit 1 to the Alphanumeric Auxiliary Readout Display Unit at the Aircraft Navigator/Communicator (NAV/COM) station. The prototype link is scheduled for installation and test aboard the P-3C update III test bed at the Naval Air Development Center (NADC), Warminster, PA. Test and evaluation of the Fiber Optic Interconnect System will be conducted over a two year flight test program.

The author wishes to acknowledge the cooperation of NADC VP Program Office, LCDR P Connor, (Code 1P1), Lockheed personnel, G Fortescue and the technical assistance and support of NOSC personnel, LCDR W J Tinston, Jr, (Code 73) and G Kosmos, (Code 924).

Released by
CL Ward, Head
Design Engineering Division

Under authority of
CD Pierson, Jr, Head
Electronics Engineering and
Sciences Department

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A prototype fiber optic interconnect system was developed to interface the CP-901 computer data processing unit 1 with the auxiliary readout display. Installation aboard a P-3C test aircraft and a proposed long term test program are discussed.

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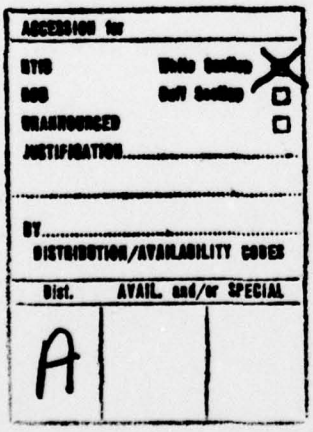

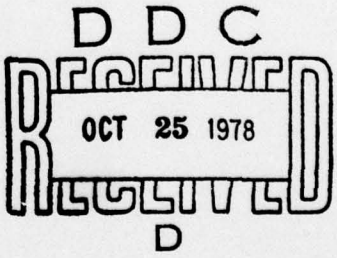

INTRODUCTION

This effort was carried out as a part of the Fiber Optic Device Technology Program and the AVIOPTICS project; the purposes are to develop, evaluate, and demonstrate the feasibility of applying fiber optic technology to naval aircraft. The goal of this effort is to evaluate the performance of a fiber optic link for alphanumeric displays aboard a P-3C aircraft. The results obtained will be utilized in the development of future fiber optic interconnect designs for naval aircraft.

P-3C NAV/COM FIBER OPTIC LINK OPERATION

The P-3C NAV/COM Fiber Optic Link was designed to handle the data transfer requirements of a cathode ray tube (CRT) alphanumeric display. In this interface (see figure 1), 18 lines of information are multiplexed into four fiber optic channels which link CP-901 data processing unit 1 (plug 1J8) to the auxiliary readout display (plug 7J2).

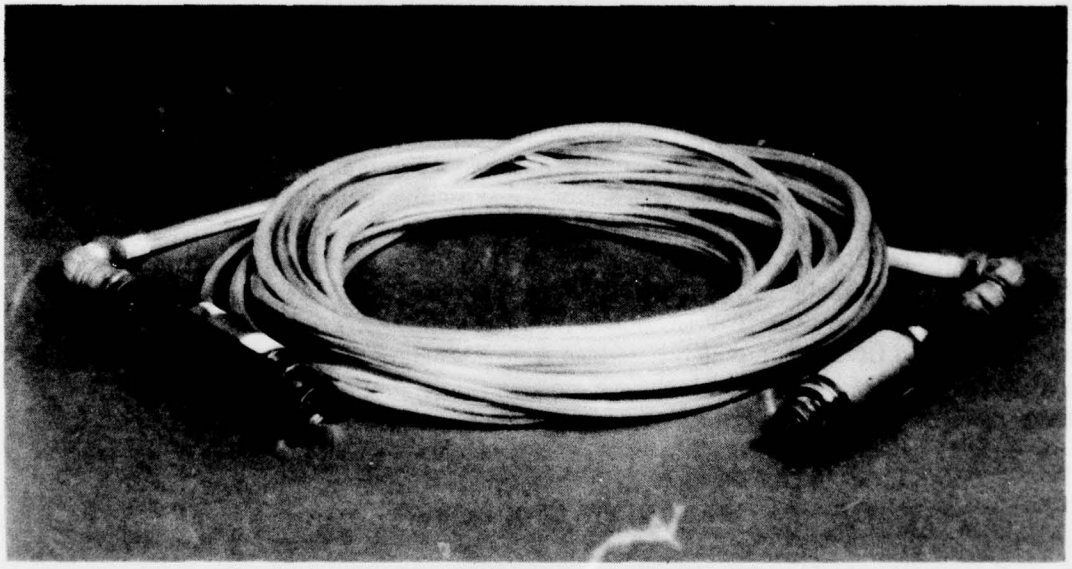

Figure 1. P-3C NAV/COM fiber optic link.

In this link, the data transfer is structured as follows:

a. 5 bits horizontal (X) deflection

b. 5 bits vertical (Y) deflection

c. 6 bits character selection

d. 1 bit CRT unblank

e. 1 bit test indicator line drive

A special alphanumeric readout display (ARD) subunit in computer data processor unit 1 is dedicated to service the requirements of the display. As shown in the block diagram of figure 2, 16 data inputs are serialized through shift registers in a conventional manner; the serialized data and a synchronizing clock signal are then transferred to the ARD unit via two fiber optic cables. The CRT unblank signal, which is repetitive every 56 μs, appears after the transmission of the multiplexed data so the deflection yokes have enough time to settle. This unblank signal is sent via a separate fiber optic channel through a separate cable.

The "test indicator" signal is a remote control for a light bulb on the CRT panel and would not ordinarily be considered for implementation with fiber optics. However, to completely eliminate potential conductive ground loop paths via the link, this signal is passed via a fourth fiber optic cable.

The CP-901 line driver outputs vary between ground (0V) and approximately +3.8 V. A line at the nominal +3.8 V level can be loaded to a level of about 50 mA peak current while maintaining approximately a 3.25 V logic level. With the 16 data lines plus the unblank line, a peak current of approximately 850 mA is available to power the fiber optic link circuitry.

Since the CP-901 computer logic is inverted (ie, ground level is logic 1 and +3.8 V is logic 0) somewhat more than a 50 percent duty cycle is available for powering the electronics, thus giving an average current of more than 425 mA. Seventeen 1N270 germanium high conductance diodes are used to channel the energy from the 17 lines to keep a small (4.7 μF) tantalum capacitor charged to nearly 3 V.

Because the fiber optic data link electronics requires about +5 V at the transmitting end (CP-901 computer end) of the fiber optic cable and a combination of plus and minus voltages at the receiving end (ARD end), a supersonic oscillator circuit is provided to drive a special toroid transformer with turn ratios selected to derive all the required operating voltages. These voltages are derived from the 3 V source obtained from the digital circuitry. Since no source of power is available at the receiving end, a small coax cable is routed along with the fiber optic cable to carry the 10 V DC power required at the ARD end. Since the coax cable carries a low level DC current, which is derived from a separate floating winding on the oscillator toroid transformer, no ground loops can exist and the immunity to electromagnetic interference (EMI) of the fiber optic data link is not compromised.

FIBER OPTIC LINK DESIGN

Generically, the benefits of implementing a fiber optic system consist of weight savings, immunity to EMI, high security and other inherent advantages of the technology. However, the concept of the Lockheed approach for the design of this link is to provide a complete stand-alone fiber optic interconnect link which is a direct replacement for the existing wire cable interconnect, without taking advantage of all the benefits that are offered by utilization of the new technology. To accomplish this goal in this feasibility model,

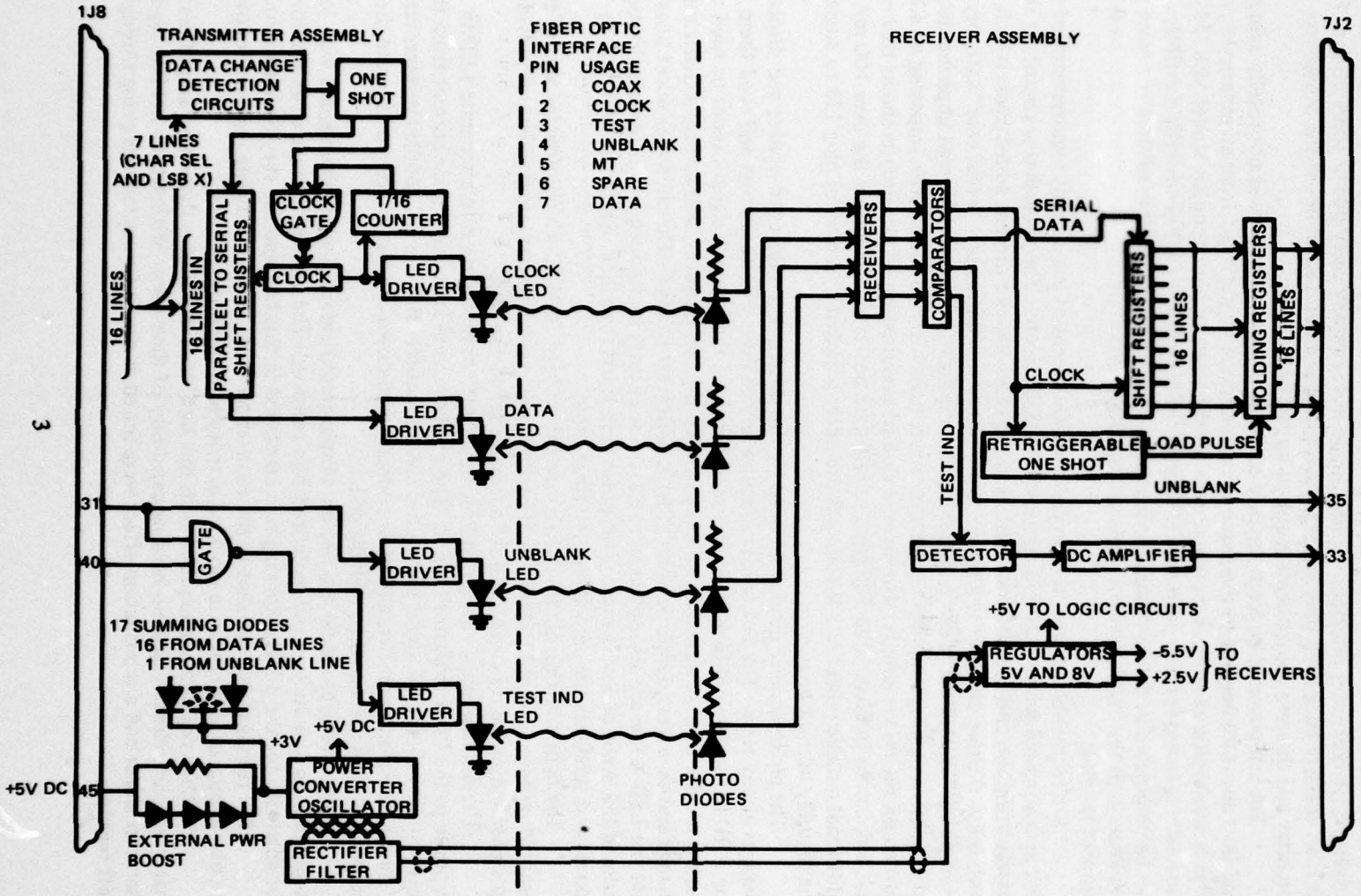

Figure 2. P-3C NAV/COM Fiber Optic Link Block Diagram.

two primary considerations had to be resolved: first, the packaging of the required electronic circuitry and the electro-optic components had to be an integral part of the link; and second, the power required by the electronic circuitry had to be supplied from circuit digital line drivers, since computer interface connectors do not normally carry power connections. For this, an oversize back-shell plug package structure was employed to house the integrated circuitry and discrete components required by the link design.

The self-powered concept initially envisioned for this design was not totally achieved, and thus about 20 percent of the required current must be provided from an external source. This is accomplished from an externally installed power supply (Acopian Model 5EB250) especially selected for this purpose. This apparent drawback is not necessarily a problem and can be eliminated in future design configurations. Since a 30 bit (30 lines) link is a more typical application of the "self powered"concept, the 30 lines will provide sufficient power to self-support the link.

It was possible to use "self power" for 80 percent of the current requirements of this link as configured with no hybrid circuits, CMOS, MSI, etc. The exclusive-or circuits at the transmitting end and the holding registers at the receiving end present added loads which, with only 17 drive lines to draw power from, places this line in the "worst case" category for "self power" operation. The "test indicator" lamp lighting circuit, although implemented in an expedient manner, requires an extra receiver, transmitter, and so forth, imposing an added burden on the power supply. However, a careful examination of the circuits shows that even this link can be implemented 100 percent self/data powered. To supply the over 100 mA of additional outside power, a 5 V source is presently required at pin 45 of plug 1J8 to augment the digitally derived power.

The alphanumeric display serviced by this data link is subject to update and display changes at any time. The link must recognize any changes of information and send them to the ARD before the unblank pulse occurs. Therefore, the unblank signal cannot be used to initiate a cycle of data serialization. Any display change, however, will involve a character change and/or a least significant bit (LSB) X deflection change. The character select lines and the LSB X line are all applied to exclusive-or circuits to produce a transfer initialization pulse in the event of any change. This pulse then starts the clock, which runs for exactly 16 counts and serializes the data across the fiber cable.

The light emitting diodes (LEDs) are driven by a 7404 IC which provides part of the required pull-up current by its own internal components. Some external pull-up is provided by separate discrete resistors to assure adequate signal rise time.

The unblank pulses are gated "on" and "off" as modulation to a separate LED in response to the "test indicator" input. The pulses require less steady state current from the power supply than a DC signal and pulses are compatible with the AC coupled receiver circuits. A simple detector, amplifier, and open collector pull-down transistor serve to generate the required lamp control at the receiving end.

Video portions of the receiver are simple amplification stages implemented with low-noise type semiconductors and metalized film resistors. The LM-319 comparators are slow but adequate for the 3 MHz clocking rate employed in this link and use very little current.

The retriggerable one shot in the receiver serves to load the holding registers following the occurrence of any new data clocking activity into the shift registers.

Holding registers are required with this link since the display deflection amplifiers and character select circuits have no holding capability of their own. Without the holding registers, character smear and a scintillation effect were noted as new information was going through the shift registers.

IMPLEMENTATION

Because of the low cost effort intended for this project, there was no attempt made to optimize the packaging of the electronics required at the transmitter and receiver ends of the link. Two oversize existing connector shells were selected to house the electronics and simplify the fiber optic/computer and fiber optic/display interfaces.

The link was essentially implemented in three sections:

a. The transmitting unit (black band)

b. The receiving unit (gray band)

c. The fiber optic cable

The transmitting and receiving units consist of three boards each containing the circuitry shown in figures 3–5 and 6–8, respectively. One end of the transmitter unit plugs into the computer connector (plug 1J8) and the other end accepts either end of the fiber optic cable. Similarly, one end of the receiver unit plugs into the auxiliary readout unit (plug 7J2) and the other end accepts the fiber optic cable.

The fiber optic cable length is longer than required; the extra length was intentionally provided to facilitate routing during installation. In addition, the cable is equipped with right angle fittings which provide a straight connection without having to bend the cable. The two fiber optic cable ends have identical clocking and are interchangeable.

TEST PLAN

The test plan for the P-3C NAV/COM fiber optic link is primarily for accumulating operating hours on the link to attempt to collect performance and mechanical integrity data on fiber optic interface systems.

The plan is to install the link on a P-3C flying test bed aircraft and monitor its performance over a period of approximately 2 years. However, since the aircraft to be used is not necessarily dedicated to testing this link, a minimum of 200 hours of operating time will be acceptable provided no catastrophic failures occur prior to accumulation of the 200 hours.

The test is to be performed at the Naval Air Development Center (NADC), Warminster, PA.

CONCLUSIONS AND RECOMMENDATIONS

Conclusions, recommendations, and test results will be published, as an addendum to this report, at the conclusion of the flight test program.

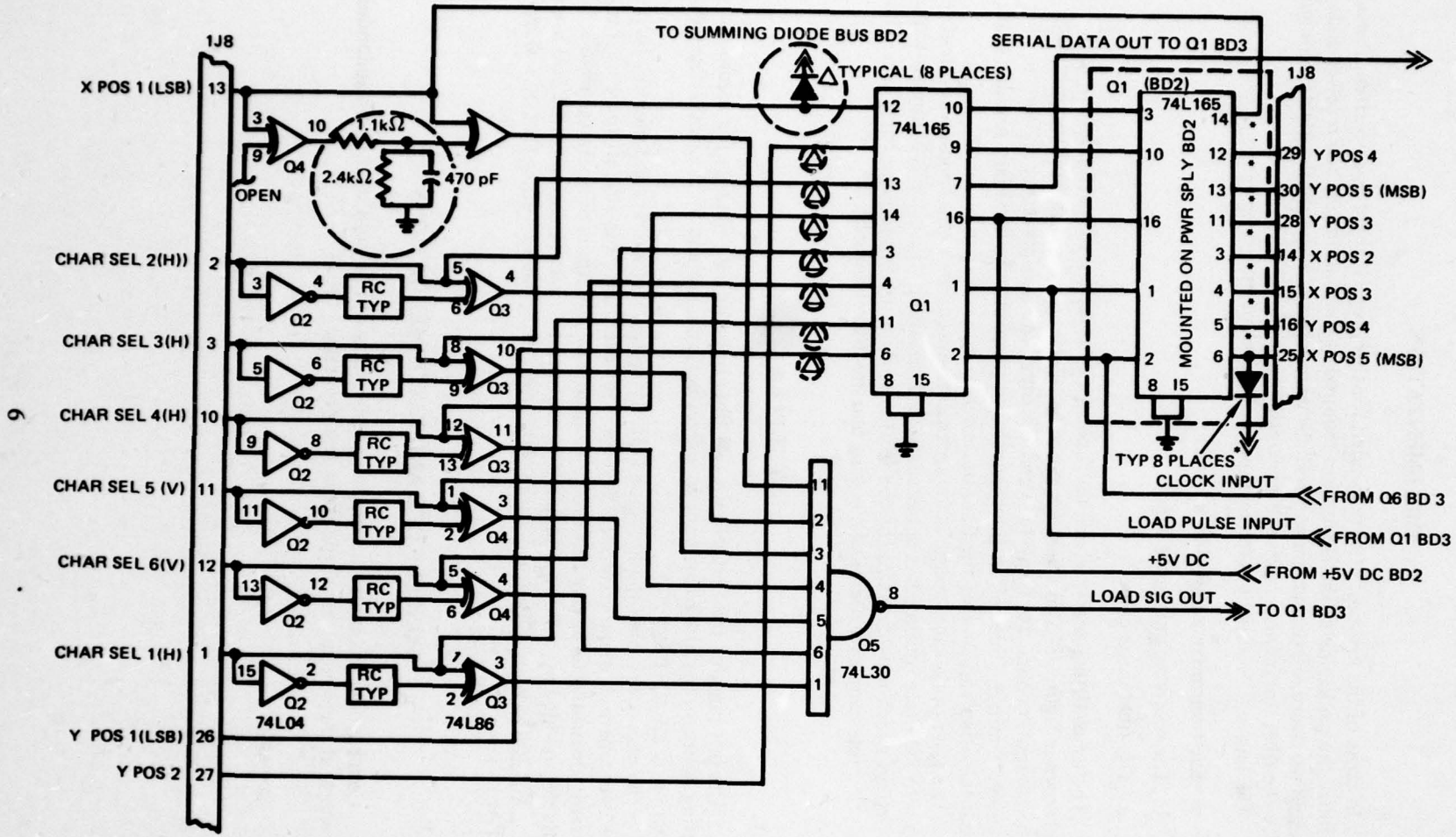

Figure 3. Transmitter Assembly Board 1.

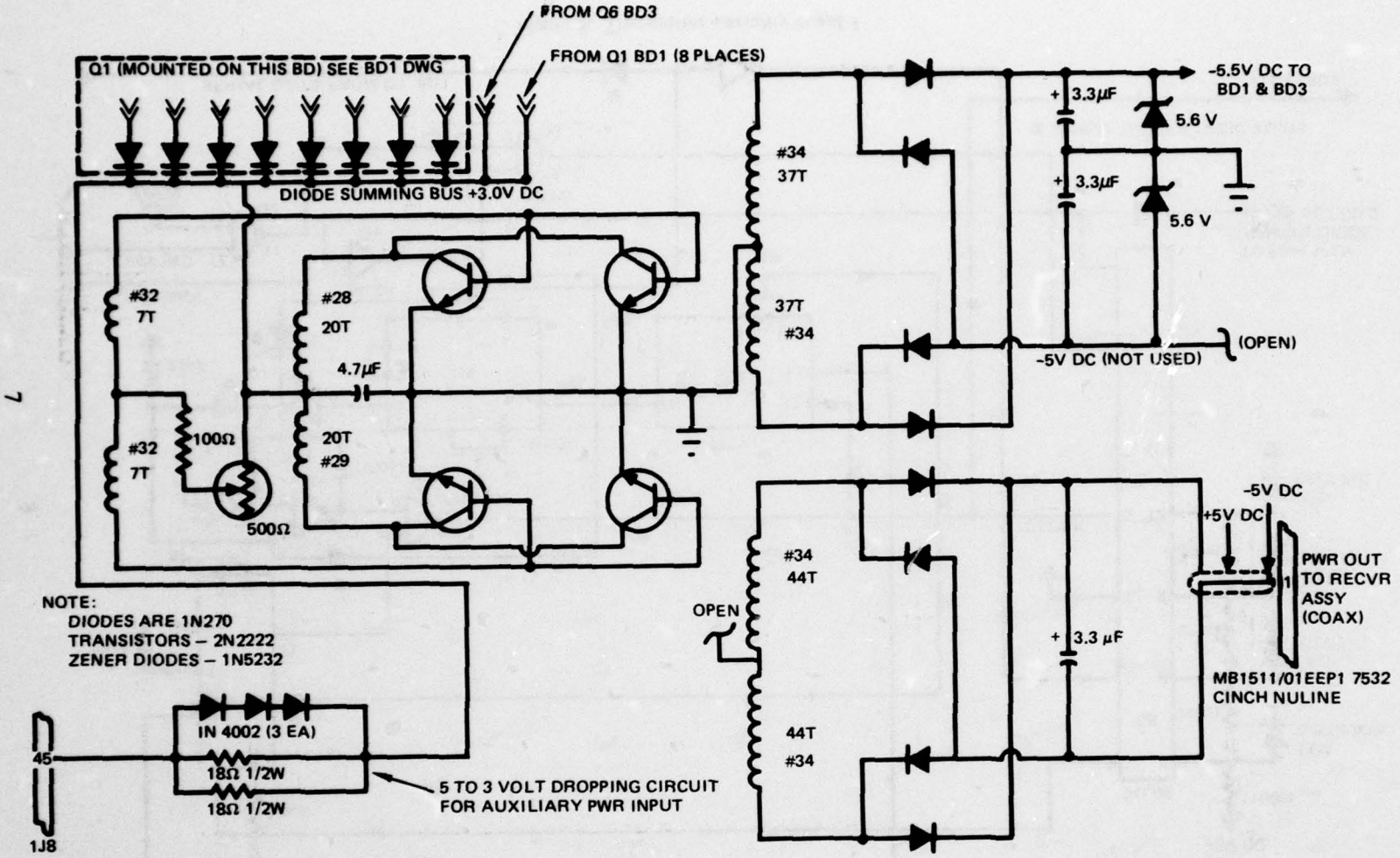

Figure 4. Transmitter assembly board 2.

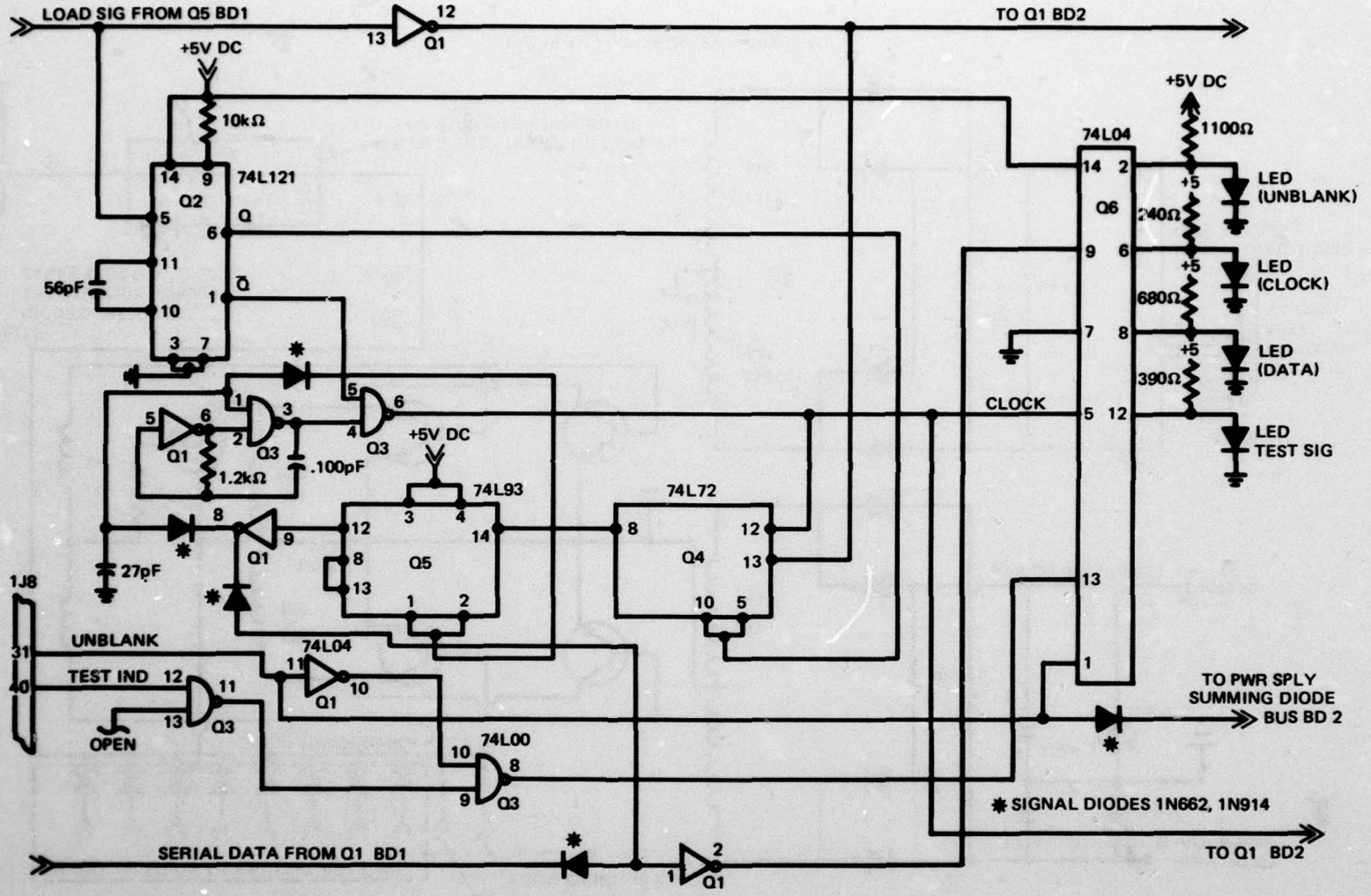

Figure 5. Transmitter assembly board 3

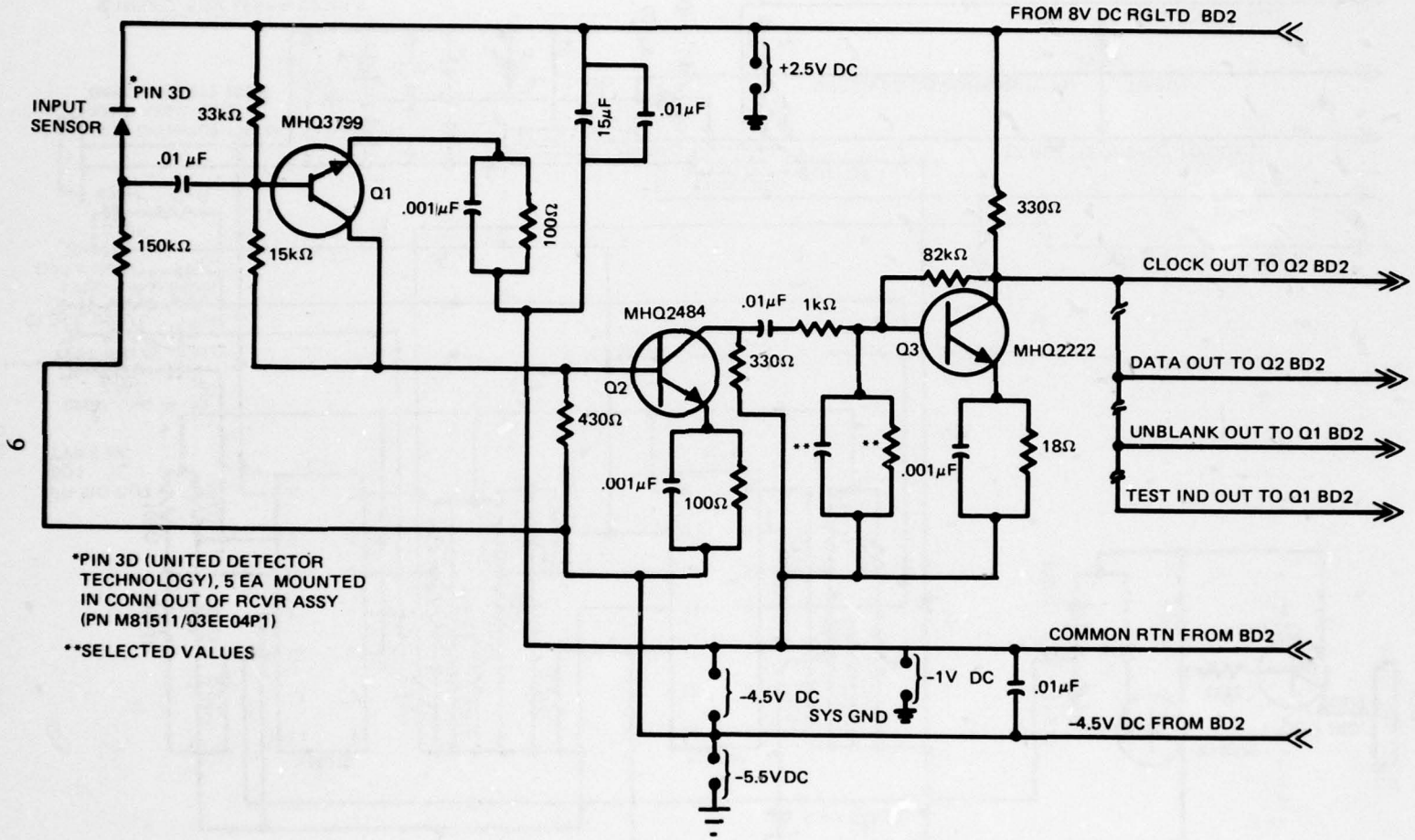

Figure 6. Receiver assembly board 1 (four each).

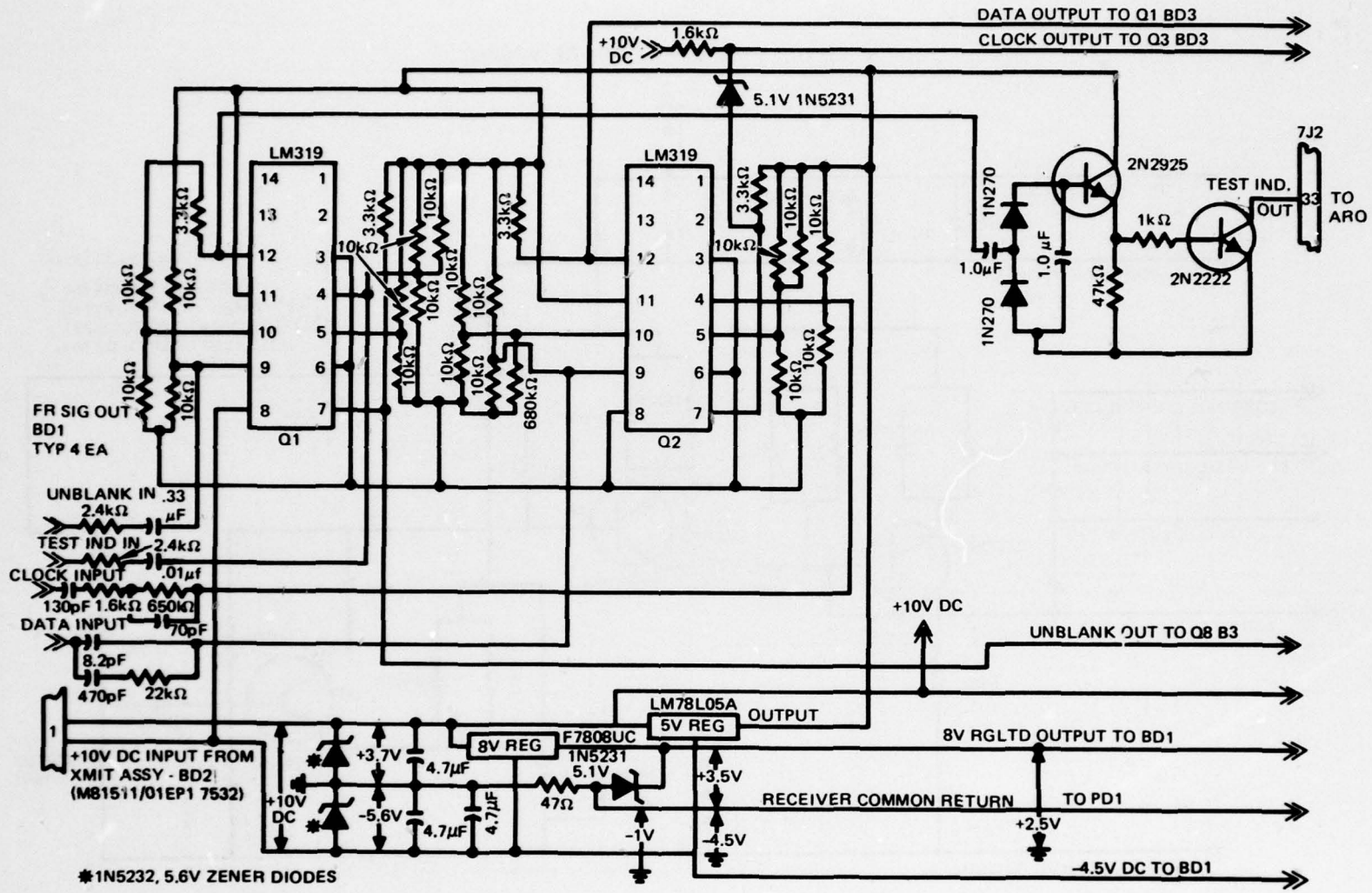

Figure 7. Receiver assembly board 2.

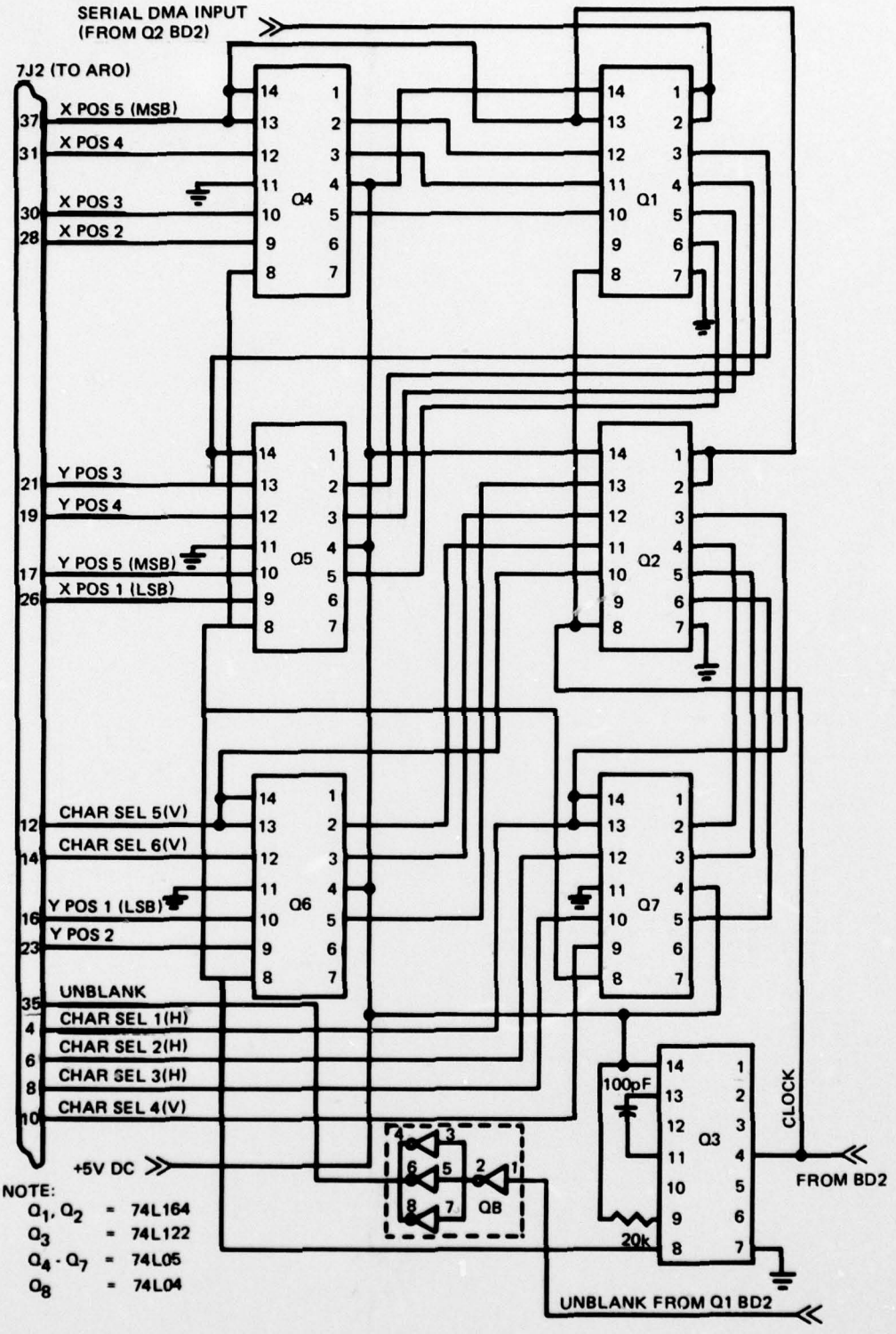

Figure 8. Receiver assembly board 3